

APPENDIX A – THE PARTIES’ PROPOSED CONSTRUCTIONS FOR EACH CLAIM TERM

No.	Term(s)	PUMA’s Construction	Defendants’ Construction
1.	“bus” all claims	No construction necessary. Alternative construction: “a signal line or set of signal lines to which a number of devices are coupled and over which information may be transferred”	“a signal line or set of parallel signal lines to which three or more devices are attached over which information may be transferred to each of the three or more devices as controlled by an arbiter”
2.	“memory bus” 164: claim 1 045: claim 4	No construction necessary. Alternative construction: “a signal line or set of signal lines to which a “umber of devices are coupled and over which information may be transferred to a memory”	“bus [as construed] that connects directly with a memory”
3.	“fast bus” 368: claim 7 045: claim 4	“bus with a bandwidth equal to or greater than the required bandwidth to operate in real time.”	<i>Indefinite</i> In the alternative: “bus [as construed] having a bandwidth sufficient to allow real time operation”
4.	“in real time” 789: claims 1, 15 315: claim 1 164: claim 1 Other elements affected by this term:	“fast enough to keep up with an input data stream”	<i>Indefinite</i> In the alternative: “fast enough to keep up with the input data stream wherein obtaining bus mastership does not consume bus cycles”

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	<p>a. “the bus having a sufficient bandwidth to enable the decoder to access the memory and operate in real time when the first device simultaneously accesses the bus”</p> <p>789: claim 1</p> <p>b. “the bus having sufficient bandwidth to transfer data in real time between the shared memory and the decoder”</p> <p>315: claim 1</p>	<p>a. “the bus having a sufficient bandwidth to enable the decoder to access the memory and operate fast enough to keep up with an input data stream when the first devices simultaneously accesses the bus”</p> <p>b. “the bus having sufficient bandwidth to transfer data in fast enough to keep up with an input data stream between the shared memory and the decoder”</p>	
5.	<p>“arbiter”</p> <p>“arbitration circuit”</p> <p>“memory arbiter”</p> <p>“arbiter circuit”</p> <p>789: claims 1, 19</p> <p>459: claims 1, 11</p> <p>194: claims 1, 11, 16, 17, 18</p> <p>368: claims 1, 5, 7, 13, 20</p> <p>045: claims 1, 4, 5, 12</p> <p>753: claims 1, 7</p> <p>164: claims 1</p>	No construction necessary.	“a component that controls direct access without multiplexing inputs”

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6.	“control circuit” 464: claims 1, 10, 19, 32	No construction necessary.	“an electronic control device that is separate from the CPU or processor and that interacts with the operating system”
7.	a. “directly supplied” 194: claim 15 368: claim 3 b. “directly supplies” 194: claim 2 368: claims 14, 21 045: claims 2, 6, 13 753: claim 3	No construction necessary. Alternative construction: a. “supplied without being stored in main memory for purposes of decoding subsequent images” b. “supplies without being stored in main memory for purposes of decoding subsequent images”	a. “supplied without intervening components” b. “supplies without intervening components”
8.	“monolithically integrated into” “integrated into” 789: claims 6, 21, 23 194: claim 19 368: claims 17, 23 045: claims 9, 15 753: claim 12 164: claim 12	“integrated into a chip with”	“formed within”
9.	a. “display device” 194: claims 1, 11, 16, 17	a. “screen and associated display circuitry”	a. “a device for displaying images or video, such as a screen”

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	368: claims 1, 7, 13, 20 045: claims 1, 4, 5, 12 753: claims 1, 7 b. “display adapter” 368: claims 2, 3 045: claim 2 753: claim 3	b. No construction necessary. Alternative construction: “a circuit for processing images”	b. “a device that processes images for a display device”
10.	“[first, second, third] onboard memor[y, ies]” 315: claim 1	No construction necessary.	“[first, second, third] memory within the decoder”
11.	a. “contiguous” b. “non-contiguous” 464: claims 1, 10, 19, 32	No construction necessary.	a. “adjacent” b. “non-adjacent”
12.	“direct memory access engine” “direct memory access (DMA) engine” “DMA engine” 464: claims 8, 17, 23 315: claim 12	No construction necessary.	“a block transfer processor that transfers data between an external device and a memory without interrupting program flow or requiring CPU intervention”

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	164: claims 9, 10		
13.	“refresh logic” 164: claims 11, 12	No construction necessary.	“logic to repeat the storage of data to keep it from becoming lost”
14.	a. “coupled” 789: claims 1, 5 368: claims 1, 7, 13, 19, 20 045: claims 1, 4, 5, 12 753: claims 1, 7 315: claims 1, 14, 15 164: claims 1, 8, 9, 11 b. “coupleable” 045: claims 1, 4, 12 753: claim 7 315: claim 1 164: claim 1 c. “coupling” 789: claim 1 194: claims 1, 16, 17	No construction necessary. Alternatively, a. “directly or indirectly connected” b. “directly or indirectly connectable” c. “directly or indirectly connecting”	Plain and ordinary meaning; no construction necessary